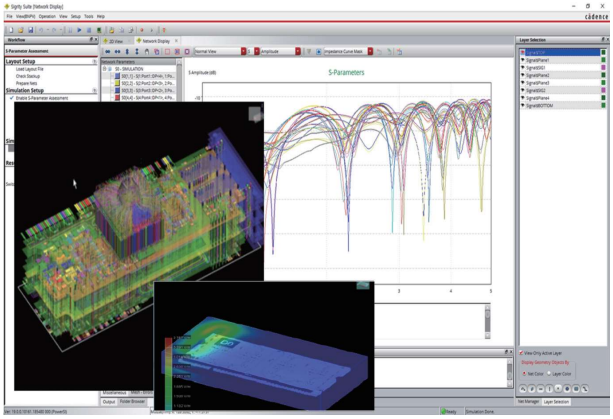
Cadence Sigrity Solutions

Cadence Sigrity SI/PI Simulation Tool은 설계된 PCB Data를 기반으로 Package, Component 등에 대해 Modeling하고 Simulation Model을 적용하여 신호반사, 왜곡, 상호간섭 등의 분석을 통해 Signal Integrity 및 Power Integrity 분석을 할 수 있는 Simulation 환경을 제공함으로써 실제 제품의 제작에 앞서 미리 동작특성을 파악할 수 있다.
또한 엄격해진 제품의 동작 사양을 만족시키기 위해 필요한 다양한 Simulation 조건도 적용하여 분석할 수 있으며 설계제품의 응용기반에 맞게 Timing 분석이나 Noise 분석과 Margin을 검증하고 실제 PCB에 적용하여 제품화함으로써 시행착오를 줄이며 제품개발 기간을 단축시킬 수 있다.

PowerSI : Frequency Domain SI/PI/EMI Simulation

PowerSI는 PCB, IC Package, SiP 등의 SSN, Signal Coupling, Target Impedance Level 등 설계 시 요구되는 Signal Integrity 및 Power Integrity 사양을 검증할 수 있는 강력한 주파수 영역 Simulation 분석환경을 제공합니다.

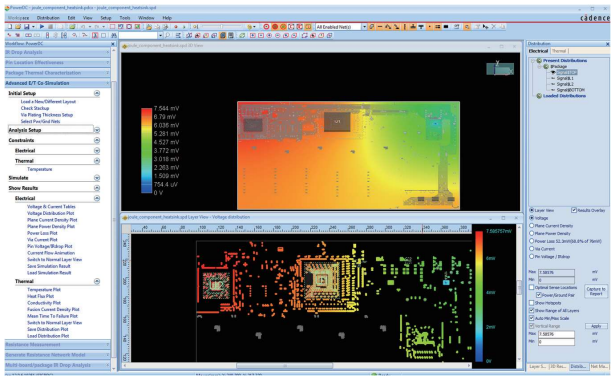


Features

- Facilitates AC analysis to assess voltage distribution across ground planes
- Establishes power delivery network (PDN) guidelines for IC packages and boards
- Evaluates electromagnetic coupling between geometries to enable better component, via, and decap placement
- Extracts frequency-dependent S, Z, and Y parameters for package and board modeling for subsequent time domain SSN simulation
- Anticipates energy leaks with near-field ration display
- Assesses decoupling capacitor strategies and verifies placement effects Enables broadband modeling including accurate DC performance characterization (patent pending)
- Integrates seamlessly with 3D solutions for IC packages and boards
- Distributed computing option accelerates analysis time (additional license required)
- Strong HSPICE flow support
- Optimized for flows with Cadence SiP Layout, Allegro® Package Designer, and Allegro PCB Designer
- Readily used in Mentor, Zuken, and Altium flows, accepting a mix of CAD databases where needed for multi-structure design support

PowerDC : IR Drop & Thermal Co-Simulation

PowerDC는 IC Package 및 PCB Design에서 IR Drop, 전류밀도 및 Thermal 분석을 빠르고 정확하게 Simulation 할 수 있으며 Electrical 및 Electrical-Thermal Co-Simulation을 통해 전류분포와 온도변화를 분석하고 Board/Package의 Thermal Distribution Analysis가 가능합니다.

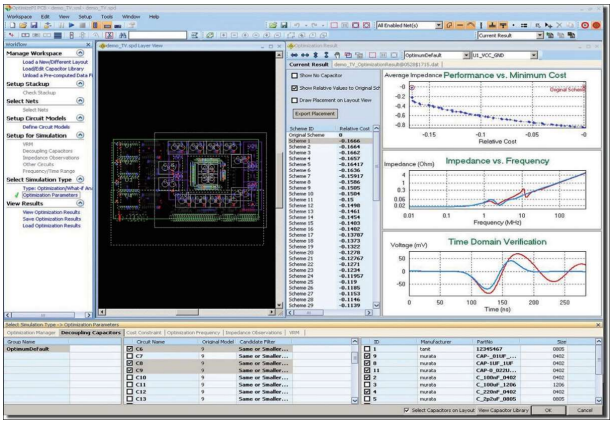


Features

- Automatically set-up DC simulations using PowerTree™ data (source/sink definitions) captured at the schematic stage of the design process
- Identifies difficult-to-locate highly resistive routing neck-downs and finds the one via among thousands that will fail under stress
- Determines if it is possible to reduce plane layers without adding DC or thermal reliability risk
- Assesses multi-structure PCB and package designs along with chip-level information
- Considers what-if improvement options with a unique block-diagram results view, and a range of visualization options,
- Easy-to-deploy workflow that is ideal for occasional users and experts alike
- Patented automation to pinpoint the best remote sense line location
- Highly accurate, even for complex designs with multiple voltage domains and complex plane structures
- Comprehensive support for multi-structure designs including stacked die, multiple boards, and all popular package types
- Visualize the power portion of your schematics with PowerTree data
- Run pre-layout simulation without copper using PowerTree data to help select components that meet design criteria
- Optimized for flows with Allegro® Package Designer Plus and its SiP Layout Option, and Allegro PCB Designer
- Readily used in Mentor, Zuken, and Altium flows, accepting a mix of CAD databases where needed for multi-structure design support

OptimizePI : Optimizing DeCAP for Impedance Issues

OptimizePI는 Board 및 IC Package에 대한 주파수 영역에서의 고도로 자동화된 PI분석을 통해 Decoupling Capacitor를 최적화할 수 있는 솔루션입니다.
Pre 및 Post Layout에서 DeCAP을 분석하고 임피던스 이슈를 확인할 수 있도록 지원합니다.

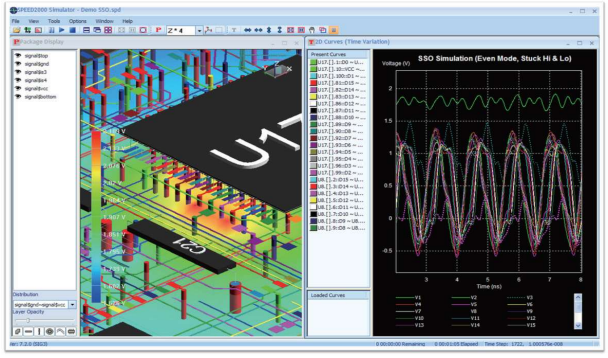


Features

- Eliminates decap over-design for PCBs and IC packages
- Reduces PDN cost for new designs and post-production products
- Develops effective decap guidelines for packaged components
- Optimizes a PDN across the board/package interface
- Identifies both the number and locations for EMI decaps
- Robust and proven underlying hybrid EM/circuit analysis technology
- Intuitive and interactive visualization of PDN performance
- Simple to set up for pre- and post-layout decap optimization
- Visualize the power portion of your schematics with Cadence Allegro® PowerTree™ data
- Capture setup information (models, net names, etc.) in a PowerTree GUI that enables assignment of target impedance constraints
- Unique device impedance and EMI resonance checking
- Ability to support large designs that include both package and board data
- Optimized for flows with Cadence SiP Layout, Allegro Package Designer, and Allegro PCB Designer
- Readily used in Mentor, Zuken, and Altium flows, accepting a mix of CAD databases where needed for multi-structure design support

SPEEDEM : Time Domain EM Simulation

SPEEDEM은 시간영역에서의 신호무결성, 전원무결성 및 ESD, EMI분석을 위한 포괄적인 PCB / Package Layout 기반 EM 시뮬레이션 툴입니다.
설계 검증 및 디버그에 대한 향상된 Layout 검증을 지원합니다.

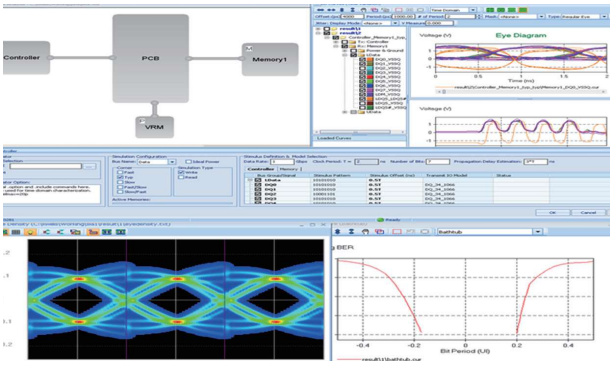


Features

- Workflows for full board screening of signal impedance, crosstalk, and return path discontinuities (no models required)
- Simulation-based SI rule checking that considers power plane noise (no models required)
- Simulates simultaneous switching noise (SSN) and identifies improvement options
- Unique electromagnetic control (EMC) simulation solution with support for designs with non-linear drivers and receivers
- Determines the impact of variations in stack-up, plane geometries, and I/O configurations
- Observes where noise is generated, identifies how it propagates, and determines if it stays within targeted levels
- Interconnect model extraction of single or coupled signal lines for use with external circuit simulators such as the Sigrity SystemSI tool
- Behaves as an FDTD-direct engine for the Sigrity SystemSI tool, enabling system-level power-aware SI analysis (no requirement for S-parameters)
- ESD workflow provides feedback on effectiveness of TVS diodes
- Optimized for flows with Cadence SiP Layout, Allegro® Package Designer, and Allegro PCB Designer
- Readily used in Mentor, Zuken, and Altium flows, accepting a mix of CAD databases where needed for multi-structure design support

SystemSI : Fastest, most advanced channel simulation

SystemSI는 High-Speed Chip to Chip 시스템 설계의 정확한 평가를 위한 포괄적이고 자동화된 신호무결성 분석 툴입니다.
강력한 병렬버스(DDRx) 및 직렬 링크 인터페이스(SATA, MIPI, PCIe 등) 구현을 보장합니다.



Features

- Accurate handling of non-ideal power delivery system influences on SI
- Concurrently evaluate SI effects such as losses, reflections, crosstalk, and simultaneous switching output (SSO)
- Support for industry-standard IBIS AMI transmitter and receiver models enable simulations of channel behavior for serial links with chips from multiple suppliers
- Highly automated measurement and reporting capabilities

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